

A Dynamic Simulation on Single Gate Junctionless Field Effect Transistor Based on Genetic Algorithm

Roya Norani¹

¹ Department of Electrical Engineering, Khorasan Institute of Higher Education University
Mashhad, Khorasan Razavi, Iran
R.Norani2014@gmail.com

Abstract

We study the I-V characteristics of single gate junctionless field effect transistor by device simulation. The sample FET is simulated at different channel lengths and the I-V curve changes due to variations of and channel length have been systematically analyzed. The new approach exhibited here utilizes a Genetic Algorithm to select the important physical and heuristic elements in order to define a compact yet precision model for Single Gate Junctionless Field Effect Transistor characteristic. The results show that the mean absolute percent error (MAPE), root-mean-square deviation (RMSD) and standard deviation error (SDE) were at an acceptable level.

Keywords: *Single Gate, Junctionless Field Effect Transistor, Device Simulation, Genetic Algorithm.*

1. Introduction

All existing transistors are based on the use of semiconductor junctions formed by introducing dopant atoms into the semiconductor material [1]. In recent years, the devices is designed which have no junctions and were made in n^+ or p^+ silicon nanowires [1]. They report full CMOS operation of gated resistors and their designed devices have full CMOS functionality, but the new designed contain no junctions or doping gradients. Among emerging devices, nanowire transistors, which could be done with the un-doped or doped body, have drawn much attention for good scaling capability and technology compatibility [2].

Currently, as MOSFET dimensions are scaled down to dozens of nanometers, the short channel effect seriously affects the behavior of devices. In the Nano-scale, the influence of short channel effect on the characteristics of conventional MOSFETs cannot be ignored. To solve this problem, a novel type of MOSFETs, named junctionless field-effect transistors, has been proposed. Compared to conventional inversion-mode MOSFETs, junctionless FETs need no p-n junction to form between regions, which can be seen as n-n-n-type (n-channel) or p-p-p-type (p-channel) junctionless MOSFET devices. It is easier to achieve a good performance of junctionless FETs fabricated on an SOI wafer. Take an n-n-n-type

junctionless FET as an example; it is turned off by piping out the electrons from the body region by the gate electric field force to make the body fully depleted at lower gate bias. The vertical channel of a VMOS is defined by the gate spacer thus the fabrication cost can be reduced drastically. The double-gate scheme of a VMOS helps to increase the gate controllability over the channel region [2]. Thinner silicon films block the channel more easily, and then the channel region achieves complete depletion. From the standpoint of the electric potential distribution, the channel energy band bends due to the reduction of the gate voltage and a strong barrier is formed between the source and drain which makes it difficult for electrons to flow from the source to drain. As the gate bias is increased, the depletion of the body region is eliminated gradually. With the increase of the electron concentration, the resistance also decreases. When the electron concentration reaches body doping concentration N_D , the channel region under the gate becomes electrically neutral. Further increasing gate voltage increases the accumulation of the electrons at the interface between the gate oxide and the silicon film. This makes the device resistance greatly reduced and form a good conductive state under a certain drain-to-source voltage. Then the device is turned on. Therefore, different from traditional n-p-n-type or p-n-p-type inversion-mode MOSFETs, junctionless FETs use majority carriers for transport between source and drain. That means it is an accumulation mode MOSFET. From the macroscopic point of view, the gate acts as a good control switch, which turns off the device at low gate bias and turns on at high gate bias on the premise that the silicon film is thin enough. This kind of device will not only assure that the device can work well like a conventional MOSFET, but also avoid the need for sharp doping concentration gradient switching from n-type to p-type. Such kind of MOSFETs greatly reduces the requirements of the fabrication process. At present, some research groups have performed some related studies of junctionless FETs, including investigating the theoretical foundations to better understand the behavior of the device [3], analysis of the turned-on characteristics of the device at different drain

voltages and the potential under various operating conditions [4].

All these above analyses are performed under the assumption that the channel length is long enough; therefore, short channel effects are ignored. Also some other investigations preliminarily studied the performances of silicon junctionless nanowire transistors in terms of short channel effects such as turn-on characteristics, output characteristics and room-temperature sub threshold slope as a function of gate voltage [5]. The junctionless VMOS is based on bulk-Si wafer. However, it is necessary to provide a more detailed study on its operating characteristics in the situation of short channel effects.

The main purpose of this work is to investigate the characteristics of short channel single gate junctionless FETs by simulations using SILVACO Atlas. There are few methods for estimating the parameters of junctionless transistor that use of optimization techniques. The component which tried to be modeled has same physical properties and these specifications tried to be modeled some mathematical ways [6], [7].

The influence on the devices' characteristics of changes in design parameters such as body doping, thickness of silicon body, and channel length has been performed systematically.

2. Properties Simulation

Figure 1 represents the schematic view of a simple single gate junctionless FET. Here, L is the channel length; t_b and t_{ox} are the thicknesses of silicon body and gate oxide, respectively. N_D and N_A represent the uniform impurity concentration for n-type and p-type FETs. The channel width is marked as W . The Source and Drain regions and body region of a junctionless FET have the same doping type and concentration. The top of the device has a gate electrode to control the device.

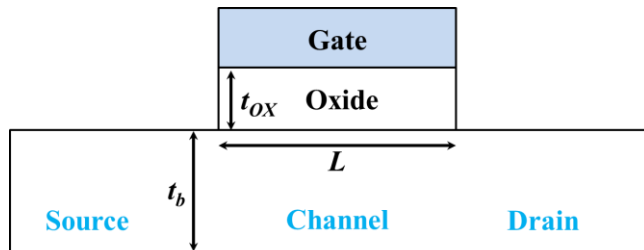


Fig. 1 Schematic view of a simple single gate junctionless FET

3. Mathematical Model

The current in N-JFET due to a small voltage V_{DS} which is, in the linear ohmic region is given by treating the channel

as a rectangular bar of material of resistivity $qN_d\mu_n$ [8]. So the current of drain-source region is defined as:

$$I_D = \frac{t_b W}{L} q N_d \mu_n V_{DS} \quad (1)$$

Where t_b is channel thickness for a given gate voltage or the thickness of silicon body. Also q is electron charge that is equals 1.6×10^{-19} C. The μ_n and N_d are electron mobility and n-type doping (donor) concentration, respectively. The drain current in the saturation region is often approximated in terms of gate bias as [8]:

$$I_{DS} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (2)$$

Where I_{DSS} is the drain-source saturation current, with this assumption the i_D is obtained with $V_{GS}=0$. We can express the I_{DSS} as:

$$I_{DSS} = \xi V_{FA}^2 = \xi_0 (1 + \varepsilon V_{DS}) V_{FA}^2 \quad (3)$$

In which the parameters are selected as $\xi_0 = 2 \times 10^{-4}$ A/V², $V_{FA} = -4$ V and $\varepsilon = 0.01$ V⁻¹. Figure 2 shows the characteristic deviation of the drain current I_D with gate-to-source voltage V_{GS} for $V_{FA} \leq V_{GS} \leq 0$.

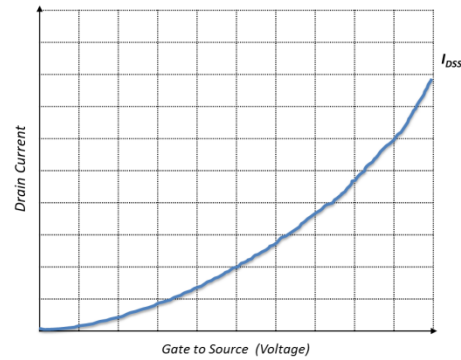


Fig. 2 I_D versus V_{GS} for Constant V_{DS} is shown in this plot

In Figure 3 the I_D versus V_{DS} is shown for eight values of V_{GS} . If the channel impure is monotonous and uniform, such that the erosion region thickness will grow in proportion to the square root of (the absolute value of) the gate-source voltage, then the channel thickness t_b can be expressed in terms of the zero-bias channel thickness a as:

$$t_b = a \left(1 - \sqrt{\frac{V_{GS}}{V_P}}\right) \quad (4)$$

Where V_P is the pinch-off voltage, the gate-source voltage at which the channel thickness goes to zero. The parameter is the channel thickness at zero gate-source voltage.

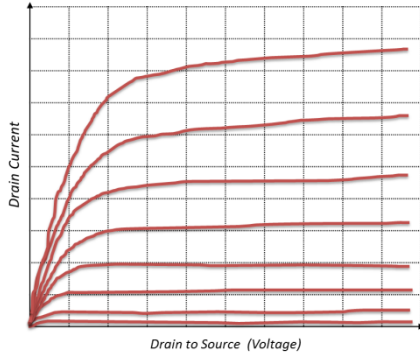


Fig. 3 I_D versus V_{DS} for Constant V_{GS} is shown in this plot

4. Genetic Algorithm

The Genetic Algorithm (GA) utilizes a non-gradient- based random search and is used in the optimization of complex systems [9]. In the algorithm, each unknown parameter is called gene and each vector of these parameters is called a chromosome [9]. The purpose of the genetic algorithm is to determine the elements of the unknown vector (chromosome) which maximizes or minimizes the defined fitness function [10]. The genetic algorithm is inspired by natural evolution and has population of individuals. In other hand individual is feasible solution to problem each individual is characterized by a Fitness function. In this optimization technique, higher fitness is better solution and based on their fitness, parents are selected to reproduce offspring for a new generation. New generation has same size as old generation; old generation dies and offspring has combination of properties of two parents. So if well designed, population will converge to optimal solution. Genetic algorithms are often applied as an approach to solve global optimization problems. In this paper we have tried to optimize the I_D versus V_{GS} . In first step, the flowchart of proposed algorithm in optimization level is shown in figure 4.

The chromosomes in the genetic algorithm are defined as a bit vector with obvious elements, where each bit relates to the model parameters. We use 13 elements where was proposed in [10] as follows:

$$\text{Chromosome_Vector} = [K \ m \ n \ V_T \ \beta \ k \ \lambda_C \ \lambda_V \ \sigma \ W_W \ W_{V_{GS}} \ p \ q] \quad (5)$$

In this vector, if a bit equal to 0, then the corresponding parameter is removed from the proposed model or we can express that n would be replaced by 2, p and q by 1, β , k , λ_V , σ , W_W and $W_{V_{GS}}$ by zero K , λ_C and V_T by their physical values. In this algorithm, two main goals have been regarded to define the target function, which are the accuracy and the complexity of the proposed model.

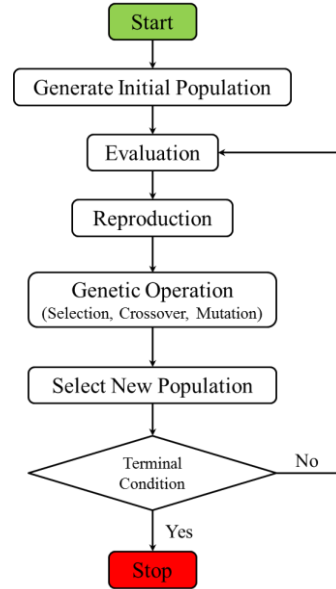


Fig. 4 The steps in genetic algorithm to determine the parameters in junctionless field effect transistor

To consider the first goal in the proposed algorithm, we define the form factor of the proposed model as follows:

$$\text{Std_Dev} = \frac{1}{N_W \times N_{V_{GS}}} \times \sum_{W=W_{\min}}^{W_{\max}} \sum_{V_{GS}=V_T}^{V_{DD}} \sqrt{\frac{\sum_{V_{DS}=0}^{V_{DD}} (I_{D_{\text{Model}}} - I_{D_{\text{Forecast}}})^2}{I_{D_{\text{Max}}}}} \quad (6)$$

Where $I_{D_{\text{Model}}}$ and $I_{D_{\text{Forecast}}}$ are the drain currents achieved by the compact model (simulated conditions) and the predicted model for same V_{DS} , V_{GS} , and W and $I_{D_{\text{Max}}}$ is the drain current at V_{DS} equal V_{GS} , N_W and $N_{V_{GS}}$ are the number of sampled width and V_{GS} used for calculating standard deviation (Std_Dev) value [11].

5. Experimental Results

We have implemented the proposed models to infer integrated results based on real state and predicted condition for junctionless field effect transistor. The proposed models were implemented in Matlab 7.1 environment and during this approach; a vector is defined with 13 elements for junctionless field effect transistor. Our goals in simulating the junctionless field effect transistor were to make them both of predict condition and real state as flexible as possible and as easy as possible to achieve relation between two approaches, especially for comparing the predict condition and real state discussed in each single gate junctionless field effect transistor.

The genetic algorithm parameters are regarded in Table 1 in which contains parameters and their values. In Figure 5, the I_D versus V_{DS} characteristics of a Single Gate JLT

transistor obtained by the proposed model and the software simulations are compared which show a very good accuracy for the proposed model.

Table 1: Genetic Algorithm Parameters and Designed Parameters of the Single Gate JLT

Genetic Algorithm		Designed Parameters of the Single Gate JLT	
Parameters	Values	Parameters	Values
Population Size	100	L	22 nm
Tournament Size	10	W	35 nm
[min_Val, max_Val]	[-5,+5]	t_{ox}	1.5 nm
Initial λ	1	t_b	15 \pm 5 nm
λ Rate	0.95	N_D	1.5 $\times 10^{18}$ cm ⁻³
Crossover Point	0.5	V_{DS}	1.2 V
Mixing Ratio	0.6	V_{GS}	0.2 V to 1.2 V
Initial Gen	13	Body Thickness	10 to 20 nm

During the simulation, the design parameters of the Single Gate JLT have to be selected as: $L = 22$ nm, $W = 35$ nm, $t_{ox} = 1.5$ nm, $t_b = 15 \pm 5$ nm, $N_D = 1.5 \times 10^{18}$ cm⁻³, fabricated on a single silicon wafer, using Silicide as the contacts. V_{DS} should be fixed at 1.2 V while the V_{GS} can be varied between 0.2 V to 1.2 V. Set the simple single gate junctionless FET's parameters as above, and the body thickness shifts from 10 to 20 nm, Figure 6 plots the comparison of the simulation results. Due to each device having the same channel length and width, the control area of the gate is the same. When the body thickness is different, the amount of majority carriers controlled by the gate is also different. Under the same lower gate bias in the sub threshold region, the more majority carriers the devices have, the more difficult it is for the depleted body region to form. Hence the threshold voltage decreases with the increasing of body thickness. The *MAPE* (Mean Absolute Percent Error) proposes the size of the error in percentage terms. It is calculated as the average of the unsigned percentage error, as shown in the (7):

$$MAPE = \frac{1}{N} \sum_{k=1}^N \frac{|F_k - A_k|}{A_k} \quad (7)$$

The root-mean-square deviation (*RMSD*) is a frequently used measure of the differences between values predicted by a model or an estimator and the values actually observed [12]. Basically, the RMSD represents the sample standard deviation of the differences between predicted values and observed values as (8).

$$RMSD = \sqrt{\frac{1}{N} \sum_{k=1}^N (F_k - A_k)^2} \quad (8)$$

Standard deviation error (*SDE*), according to (9), indicates the persistent error even after calibration of the model.

$$SDE = \sqrt{\frac{1}{N} \sum_{k=1}^N \left(\frac{|F_k - A_k|}{A_k} - \frac{MAPE}{100} \right)^2} \quad (9)$$

Errors in modeling with considering *MAPE*, *RMSD* and *SDE* are summarized in Table 2.

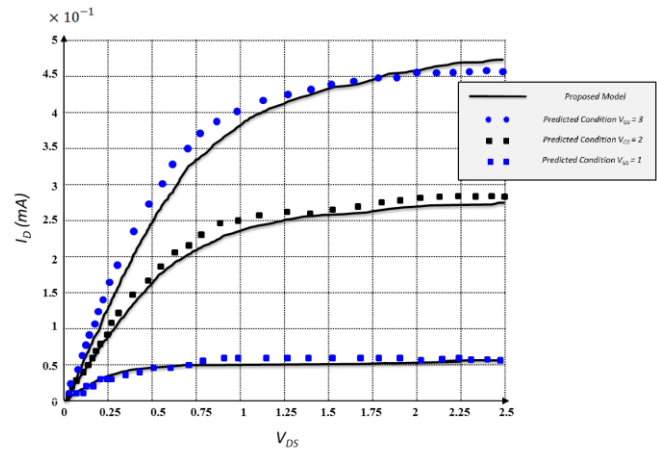


Fig. 5 The I_D versus V_{DS} is shown that contains characteristic of Single Gate JLT

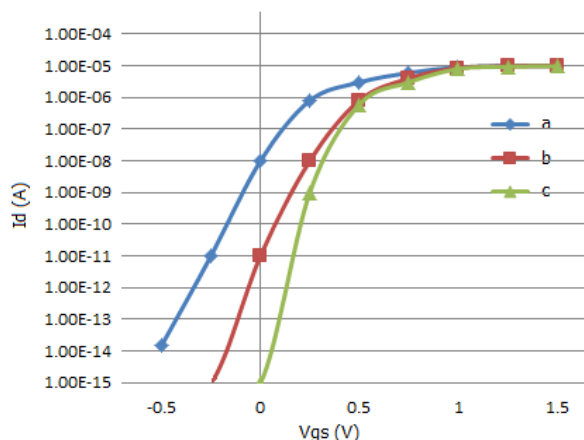


Fig. 6 Influence of body thickness for simple single gate junctionless FETs.
(a) $t_b = 10$ nm, (b) $t_b = 15$ nm and (c) $t_b = 20$ nm

Table 2: Calculation of MAPE, RMSD, SDE and Precision of the proposed technique

Error Criteria			
MAPE (%)	RMSD	SDE	Precision (%)
0.5708	0.0128	0.0379	96.42
0.8461	0.0172	0.0510	95.15
1.5545	0.0197	0.0583	94.44
1.9079	0.0637	0.1406	94.09
1.3717	0.0645	0.1425	93.62
2.0675	0.0657	0.1459	92.93
1.8614	0.0601	0.1332	93.13
2.9326	0.0595	0.1336	92.06
2.6511	0.0594	0.1346	91.34
2.3696	0.0594	0.1361	90.63
2.3842	0.0682	0.1532	91.61
2.0926	0.0695	0.1570	90.90
2.0881	0.0596	0.1382	89.91
2.5671	0.0597	0.1400	89.43

6. Conclusion

In this paper the characteristics of a simple single gate junctionless FET was simulated and finally these factors were analyzed. This paper analyzed the influence of body thickness on the threshold voltages and the Drain Current at different Gate voltages. In next step by using Genetic algorithm, one can select between the thirteen proposed model elements based on the precision that needed for a specific objective. For the precision regarded in this paper, only 9 elements were considered and so notified in the simulations.

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